Akshay Prasad

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PROFESSIONAL SUMMARY

Results-driven GPU RTL Hardware Engineer with 5+ years of experience specializing in high-performance GPU architecture, RTL design, and top-tier quality assurance. Proven track record of delivering complex projects on time by collaborating with cross-functional teams to develop and innovate cutting-edge hardware solutions.

CORE COMPETENCIES

Technical Proficiency: RTL Design, RTL Quality, GPU Architecture, ASIC Design flow, Design Automation and Testing, Artificial Intelligence (AI) for enhancing design workflows and automation

Programming Languages: Verilog, SystemVerilog, Python, Tcl, Perl, C

Tools: Synopsys VCS, VC SpyGlass (LINT, CDC), Formality, Design Compiler (DC), Fusion Compiler (FC), Cadence Xcelium (xrun), Perforce, Git, Mentor Graphics ModelSim, Cadence Innovus, VS Code, Cursor, Copilot, Google Gemini, OpenAI ChatGPT

PROFESSIONAL EXPERIENCE

GPU RTL Integration Engineer — *Jan 2023 – Present*

Samsung, San Jose, CA

- Developed and validated multiple GPU top-level configurations to meet specific performance requirements. Managed the RTL database via Perforce and led cross-functional design bring-up.
- Guided floorplan-driven connectivity for Multiple Instance Modules (MIM) and unique tiles to optimize feed-through routing, reduce global congestion, and minimize layout synthesis effort for the PD team. Mapped the logical daisy-chaining of debug buses, SLM telemetry (ProteanTecs), and memory power controls directly to physical tile placement.
- Developed, owned, and maintained Jenkins regression jobs for RTL quality sign-off, executing VCS, Xcelium (xrun), LINT, CDC, DC/FC elaboration, and SG-DFT checks. Conducted formal equivalence checking (LEC) to validate logical vs. tiled and behavioral vs. structural netlists.
- Delivered high-quality RTL to Physical Design and SoC teams, providing essential design collateral (including UPF and IP-XACT) to ensure efficient hand-offs and seamless integration, while collaborating closely with DV and Emulation teams to secure sign-off prior to milestone releases.
- Partnered with Synopsys engineers to upgrade LINT and CDC tool versions and refine ruleset tags, proactively improving design methodologies. Developed custom Python and Perl scripts to automate regression runs and streamline workflow tasks.

Design Automation Engineer — *June 2020 – Jan 2023*

Intel, Hillsboro, OR

- Defined and implemented verification scripts and flows using Python and Perl, including automated quality checks and flow optimizations, ensuring MPS product design seats met full-chip tape-out requirements with high accuracy.
- Developed CAD automation tools for physical design verification, including Design Rule Check (DRC), layout synthesis, and validation, enhancing design accuracy and efficiency.
- Designed die-rings (Etch-ring, EDM, and PRS) for various die sizes and filler seats for multi-node technologies, supporting the Shuttle program.
- Provided comprehensive customer support during tape-out executions, assisting with design rules, layout collaterals, and requirements.

ACADEMIC EXPERIENCE

Graduate Teaching Assistant | EEE 525 - VLSI Design — ***Jan 2020 - May 2020***
Arizona State University (M.S. Electrical Engineering), Tempe, AZ

Graduate Teaching Assistant | EEE 433/591 - Analog Circuit Design — ***Aug 2019 - Dec 2019***
Arizona State University (M.S. Electrical Engineering), Tempe, AZ

Graduate Service Assistant | EEE 498/591 - Python for Rapid Engineering Solutions — ***Jan 2019 - Jul 2019***
Arizona State University (M.S. Electrical Engineering), Tempe, AZ